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APPLICATION FOR LETTERS PATENT

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Plasma Etching Process And Chemical Vapor
Deposition Process Of Depositing A Material Over
A Semiconductor Substrate

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1 Plasma Etching Process And Chemical Vapor Deposition Process Of
2 Depositing A Material Over A Semiconductor Substrate

3 TECHNICAL FIELD

4 This invention relates to plasma etching processes and to chemical
5 vapor deposition processes of depositing materials over semiconductor
6 substrates.

8
9 BACKGROUND OF THE INVENTION

10 In the processing of integrated circuits, electrical contact is
11 typically made to isolated active device regions formed within a wafer
12 substrate typically comprising monocrystalline silicon. The active regions
13 are typically connected by high electrically conductive paths or lines
14 which are fabricated above an insulative material formed over the
15 substrate surface. Further, electrical contact is also typically made to
16 other conductive regions received outwardly of the wafer, such as to
17 conductive lines, contact plugs and other devices. To provide electrical
18 connection between two conductive regions, an opening in an insulative
19 layer is typically etched to the desired regions to enable subsequently
20 formed conductive films to make electrical connection with such regions.

21 The drive for integrated circuits of greater complexity, performance
22 and reduced size has driven designers to shrink the size of devices in
23 the horizontal plane. Yet to avoid excessive current density, the
24 horizontal scaling has not necessarily been accompanied by a reduction

1 in the vertical dimension. This has resulted in an increase of the ratio
2 of device height to device width, something generally referred to as
3 aspect ratio, and particularly with respect to contact openings.

4 Increased aspect ratio can result in difficulties in the overall
5 etching process typically used to etch openings through insulative
6 materials for making an electrical contact. For example, one common
7 insulating material within or through which electrical contact openings
8 are etched is borophosphosilicate glass (BPSG). A typical process for
9 etching a contact opening in such material includes dry anisotropic
10 etching, with or without plasma. The ever increasing aspect ratios of
11 contact openings has been accompanied by undesired deposits or residue
12 remaining behind on the sidewalls or base of the contact openings at
13 the conclusion of the etch. This residue is typically in the form of a
14 tenacious and insulative carbon polymer derived from one or both of
15 photoresist which is undesirably removed during the etch or the etching
16 gases themselves used to etch the contact opening through the insulator.
17 The insulative residue at best reduces the contact area available for the
18 desired region to which electrical connection is to be made. At worst,
19 it can completely occlude subsequently deposited conductive material
20 from making suitable electrical contact with the desired region. Residue
21 material might also be present in the form of native silicon dioxide and
22 sub-stoichiometric oxide. Such can by themselves increase contact
23 resistance, particularly with sub-stoichiometric oxide which adversely
24 affects silicidation when forming silicide contacts.

1 While the invention was principally motivated and resulted from
2 achieving solutions to the above-identified problems, the invention is not
3 so limited, with the scope being defined by the accompanying claims as
4 literally worded and interpreted in accordance with the Doctrine of
5 Equivalents.

6 7 8 SUMMARY OF THE INVENTION

9 The invention comprises plasma etching processes and chemical
10 vapor deposition processes of depositing a material over a semiconductor
11 substrate. In one implementation, a plasma etching process comprises
12 forming a carbon containing material over a semiconductor substrate.
13 The carbon containing material is plasma etched from the substrate at
14 a temperature of at least 400°C using a hydrogen or oxygen containing
15 plasma.

16 In one implementation, a plasma etching process includes forming
17 a masking layer over a substrate. The masking layer is patterned to
18 form openings therein. Material beneath the masking layer is etched
19 through the openings. After such etching, the masking layer is removed
20 from the substrate. After such removing and before subsequently
21 depositing any material over the substrate, the substrate is plasma
22 etched at a temperature of at least 400°C.

23 In one implementation, a semiconductor plasma etching process
24 comprises first etching material from a substrate and forming an

1 undesired residue at least partially over the substrate during the first
2 etching. After the first etching and before subsequently depositing any
3 material over the substrate, the undesired residue is plasma etched from
4 the substrate.

5 In one implementation, a chemical vapor deposition process of
6 depositing a material over a semiconductor substrate comprises
7 positioning a semiconductor substrate within a plasma enhanced chemical
8 vapor deposition reactor. The substrate is plasma etched within the
9 reactor using a first gas chemistry. After the plasma etching, a
10 material is chemical vapor deposited over the semiconductor substrate
11 within the reactor using a second gas chemistry without removing the
12 substrate from the reactor between the etching and the depositing.

13 In one implementation, a method of forming a conductive contact
14 includes forming an insulative material over a silicon comprising
15 substrate. An opening is formed into the insulative material over a
16 node location on the silicon comprising substrate to which electrical
17 connection is desired. First plasma etching is conducted within the
18 opening using a gas chemistry comprising hydrogen and exposing silicon
19 of the substrate to said plasma hydrogen. After the first plasma
20 etching, second plasma etching is conducted within the opening using a
21 gas chemistry comprising chlorine. After the second plasma etching, a
22 silicide material is formed within the opening in contact with silicon of
23 the substrate.
24

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic fragmentary view of a semiconductor wafer fragment at one processing step in accordance with the invention.

Fig. 2 is a view of the Fig. 1 wafer at a processing step subsequent to that shown by Fig. 1.

Fig. 3 is a view of the Fig. 1 wafer at a processing step subsequent to that shown by Fig. 2.

Fig. 4 is a view of the Fig. 1 wafer at a processing step subsequent to that shown by Fig. 3.

Fig. 5 is a view of the Fig. 1 wafer at a processing step subsequent to that shown by Fig. 4.

Fig. 6 is a view of the Fig. 1 wafer at a processing step subsequent to that shown by Fig. 5.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Referring to Fig. 1, a semiconductor wafer fragment is indicated generally with reference numeral 10. Such comprises a bulk monocrystalline silicon semiconductor substrate 12 having an exemplary

1 | conductive diffusion region 14 formed therein. In the context of this
2 | document, the term "semiconductor substrate" is defined to mean any
3 | construction comprising semiconductive material, including, but not limited
4 | to, bulk semiconductive materials such as a semiconductive wafer (either
5 | alone or in assemblies comprising other materials thereon), and
6 | semiconductive material layers (either alone or in assemblies comprising
7 | other materials). The term "substrate" refers to any supporting
8 | structure, including, but not limited to, the semiconductive substrates
9 | described above.

10 | An electrically insulative layer 16, such as BPSG, is formed over
11 | substrate 12. A masking layer 18 is formed thereover. An example
12 | and preferred material for layer 18 is photoresist, whereby
13 | photolithography will be utilized to pattern a contact opening to
14 | diffusion region 14. Any other masking layer, whether conductive or
15 | insulative, is contemplated, with silicon dioxide and silicon nitride being
16 | examples utilized alone or in combination with other overlying masking
17 | layers. Further, no masking layer might be utilized.

18 | Referring to Fig. 2, masking layer 18 is patterned to form
19 | openings therein (preferably therethrough), such as illustrated opening 20
20 | over diffusion region 14.

21 | Referring to Fig. 3, layer 16 beneath masking layer 18 through
22 | opening 20 is etched from the substrate. Such etching is preferably a
23 | dry anisotropic etch, with or without plasma, and is conducted to form
24 | an opening 21 and outwardly expose region 14, and is conducted

1 substantially selective relative to layer 16 and region 14. An example
2 dry etching gas chemistry would include carbon and halogen components,
3 with CF_4 being but one example. Wet or other etching could also be
4 conducted, but the invention is described principally with respect to the
5 above Background section-described problem which motivated the
6 invention. Etching in the described or other manners can undesirably
7 produce residue or deposits 22 at least partially over the substrate
8 during the first etching, such as within the base of the contact opening
9 as shown. Such are typically in the form of carbon containing polymers
10 resulting from one or both of photoresist material undesirably removed
11 during the etch or from the etching gases themselves.

12 The above-described and depicted processing is but one example
13 whereby some material is etched from a substrate and an undesired
14 residue is formed at least partially over the substrate during the etch.
15 Such also is but one method of forming a carbon containing material
16 over a semiconductor substrate. Alternate etchings which form a
17 residue and alternate methods of forming carbon containing materials
18 are of course contemplated. By way of example only, a carbon
19 containing material might be formed over a semiconductor substrate by
20 a deposition, cleaning, other etching or other processes. Further by way
21 of example only, an undesired residue which may or may not be a
22 carbon containing polymer could be formed over the substrate by other
23 etching processes, including but not limited to wet or dry etching and
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1 etching process where conductive materials are being etched to form
2 conductive lines or other device components.

3 Referring to Fig. 4, masking layer 18 has been removed from the
4 substrate after the etching to produce opening 21.

5 Referring to Fig. 5 and preferably before subsequently depositing
6 any material over the substrate, plasma etching of the substrate is
7 conducted. Preferably, such plasma etching is conducted to remove the
8 undesired residue from the substrate, and more preferably is conducted
9 to be selective relative to removal of layer 16 and all other exposed
10 material of the wafer. The plasma etching is preferably conducted at
11 a temperature of least 400°C, and even more preferably at a
12 temperature of at least 600°C. Further, the temperature is preferably
13 not allowed to rise above 800°C. Pressure is preferably maintained at
14 from 1 mTorr to 10 Torr. The plasma preferably contains hydrogen or
15 oxygen which in the case of a carbon containing material, such as a
16 residue comprising a carbon polymer, is effective and substantially
17 selective in removing such material from the substrate relative to the
18 typical oxide and silicon materials on the wafer. Hydrogen or oxygen
19 containing plasmas could be utilized alone, or the plasma might
20 comprise some suitable combination. Preferably, the hydrogen containing
21 plasma is derived at least in part from one or both of H₂ and NH₃.
22 Further, the plasma can predominately comprise hydrogen. Example
23 oxygen containing plasmas can be derived from, for example, O₂ and
24

1 O₃. The plasma might also contain other reactive or inert gases, with
2 Ar being but one example.

3 A specific example process utilized a 6-liter Applied Materials
4 Centura 5200TM single-wafer reactor, which is a parallel plate capacitively
5 coupled reactor. Preferred power in accordance with an aspect of the
6 invention using such a reactor is from 100 to 1000 watts, with 300
7 watts being utilized in this example. Wafer temperature was maintained
8 at 635°C, with reactor pressure being held at 1.5 Torr. The gas flow
9 to the reactor was H₂ and Ar at respective flow rates of 2000 sccm
10 and 1000 sccm. The etch was conducted on a wafer comprising a
11 carbon polymer containing residue derived from a previous dry
12 anisotropic etch of BPSG relative to a monocrystalline silicon substrate,
13 with in this example a contact opening having an aspect ratio of 8:1
14 having previously been etched. The subsequent plasma etching was
15 conducted for 30 seconds, and selectively removed the carbon containing
16 polymer from the substrate relative to the otherwise exposed oxide and
17 silicon materials.

18 One preferred implementation of the invention comprises
19 conducting such plasma etching within a plasma enhanced chemical vapor
20 deposition reactor just prior to chemical vapor depositing of a film over
21 the wafer in such reactor with or without plasma. In a preferred
22 implementation, a semiconductor substrate is positioned within the
23 plasma enhanced chemical vapor deposition reactor. The substrate has
24 some residue such as a carbon containing polymer formed at least

1 partially thereover, and typically as the result of previous processing, for
2 example in other equipment (i.e., the substrate of Fig. 4). Plasma
3 etching of the substrate is conducted within the reactor using a first gas
4 chemistry, for example, the chemistries and conditions described above
5 (i.e., to produce the result of Fig. 5.) After the plasma etching, a
6 material is deposited, for example chemical vapor deposited with or
7 without plasma, over the semiconductor substrate within the reactor
8 using a suitable second deposition gas chemistry without removing the
9 substrate from the reactor between the etching and the depositing (i.e.,
10 to produce a layer 24 such as shown in Fig. 6). Where the plasma
11 etching and chemical vapor depositing are conducted both
12 subatmospheric, the substrate is preferably not exposed to atmospheric
13 or higher pressure conditions intermediate the plasma etching and the
14 depositing. Example preferred materials for filling contact opening 21
15 include silicides at the base of the contact and overlying polysilicon or
16 tungsten. The silicide can be formed, by way of example only, by
17 refractory metal deposition and anneal, or by chemical vapor deposition
18 directly of the silicide.

19 When etching with hydrogen after contact formation over a silicon
20 containing substrate in accordance with an aspect of the invention, it
21 has been discovered that silicide contacts at the base of the opening
22 can have less than optimum conductivity. Apparently, a tenacious
23 hydrogen-silicon bond can form on the silicon from the plasma
24 treatment. Such can lead to formation of overly thin silicide in these

1 portions, thus leading to increased resistance. Accordingly, a preferred
2 additional plasma etching is conducted using another gas chemistry
3 (preferably comprising chlorine, or hydrogen and chlorine) intermediate
4 the etching with the first gas chemistry and depositing with the second
5 gas chemistry. The chlorine is preferably derived from one or both of
6 Cl_2 and HCl . Hydrogen might also be present from H_2 .

7 Using the above described 6-liter reactor as an example, preferred
8 power is from 100 to 1000 watts, with 200 watts being a specific
9 example. Wafer temperature is preferably maintained between 200°C
10 and 800°C , with 200°C and 400°C being specific examples. Pressure is
11 preferably maintained between 1 mTorr and 100 Torr, with 5 Torr being
12 a specific example. An example gas flow would be 100 sccm of Cl_2
13 and 100 sccm of Ar. Where hydrogen is also being fed to the reactor,
14 preferably at least 10% of the reactive gas flow will comprise hydrogen.
15 One specific example would be a 1:1 volumetric flow ratio of H_2 to
16 Cl_2 . Etching time is preferably between 5 seconds and 30 seconds.
17 Reduction to practice examples showed increased thickness of the silicide
18 which was formed subsequently, increased conductivity, and lower
19 chlorine and oxygen incorporation in the films after treatment with a
20 chlorine containing plasma.

21 In compliance with the statute, the invention has been described
22 in language more or less specific as to structural and methodical
23 features. It is to be understood, however, that the invention is not
24 limited to the specific features shown and described, since the means

1 herein disclosed comprise preferred forms of putting the invention into
2 effect. The invention is, therefore, claimed in any of its forms or
3 modifications within the proper scope of the appended claims
4 appropriately interpreted in accordance with the doctrine of equivalents.
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